**MOUNT ZION COLLEGE OF ENGINERING, KADAMMANITTA**

**SECOND INTERNAL MCA DEGREE EXAMINATION, NOVEMBER 2019**

**FIRST SEMESTER**

**COURSE COD: RLMCA109**

**COURSE NAME: DIGITAL FUNDAMENTALS**

**Answer key**

**Max.marks:30 Duration: 1:30 Minutes**

**Part A**

***Answer all questions, each carries 3 marks***

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| 1. Explanation of combinational logic circuits (1.5 marks) sequential logic circuits. (1.5 marks) | CO3 |
| 2. Explanation of Asynchronous counters (3 marks) | CO3 |
| 3. Explanation of parity generator and checker. (3 marks) | CO3 |
| 4. Explanation of flip-flop.(2 marks) explanation of bistable multivibrator(1 mark) | CO3 |

**Part B**

***Answer one question from each module and carries 6 marks***

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| 5. Description of 8X1 multiplexer withtruth table and circuit - 2marks  Representing the expression F(W,X,Y,Z) as truth table - 2 marks  Designing a circuit with X,Y,Z connected to selection lines - 2marks  . | CO4 |

OR

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| 6. Explanation of full adder(2 marks) and working (4 marks) | CO4 |

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| 7. Truth table of D flipflop - 1 mark  Excitation table of RS flipflop - 2 mark  Combine the tables of RS and D flipflop [conversion table] - 1mark  Circuit diagram - 2mark | CO4 |

OR

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| 8. Logic symbol of JK flipflop - 1mark  Truth table of JK flipflop - 1marks  Circuit diagram 2 marks  Description of JK flipflop - 2 marks | CO4 |

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| 9. Asynchronous counter definition- 1 mark  4 bit Asynchronous counter description - 4mark  Timing diagram(1 mark) | CO4 |

OR

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| 10. Types of shift register - 2 marks  Explanation of any one shift register – 4 marks | CO3 |